

Estimating the Power Quality disturbance caused by Personnel Computer

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ABSTRACT

Personal computers draw non-sinusoidal current with odd harmonics more significantly. Power Quality of distribution networks is severely affected due to the flow of these generated harmonics during the operation of electronic loads. Switch-mode power supplies (SMPS) are one of the most vital part of PC, typically found in large numbers in modern power supply systems. These devices usually draw non-linear current and are, therefore, significant sources of harmonics. Although it is well known that the presence of harmonics will result in negative effects (e.g. higher thermal stresses and overloading, or increased neutral conductor currents), the assessment of the actual harmonic levels is not a simple task. Harmonic emission of individual SMPS will vary based on the differences in their circuits and operating conditions. As a consequence, these variations result in the harmonic emission of the harmonics, which is analysed in detail in this paper. Validation of the load models is done by performing case study for an industrial supply system and comparing the THDs obtained from simulation using MATLAB with the THD values obtained by measurement.

Index Terms— Component-based load modelling, Load aggregation, Harmonics, Switch-mode power supply.

1.0 INTRODUCTION

RECENT development of the consumer electronics market resulted in significantly increased numbers of modern electronic equipment connected to low-voltage power supply systems (e.g. personal computers, laptops, televisions, CD/DVD players, etc.). This equipment is sensitive to voltage variations and requires a regulated dc voltage supply, commonly referred to as a 'switch-mode power supply' (SMPS) [1]. It is estimated that power electronic loads are now responsible for around 30% of the total demand in the Indian residential load sector, and it is anticipated that their contribution in the future will further increase[2]. Although the analysis of the SMPS loads in this paper focuses mainly on the residential load sector, the general conclusions are to a large extent also applicable to the other load sectors where SMPS category of loads is prevalent, i.e. commercial load sector. The nature of

operation of SMPS load results in a nonlinear current waveform being drawn from the power supply system. This is due to the charging/discharging of the dc link capacitor (C_{dc} , Fig. 1), which is used to reduce (i.e. to "smooth") the variations of the bridge rectifier dc voltage output.

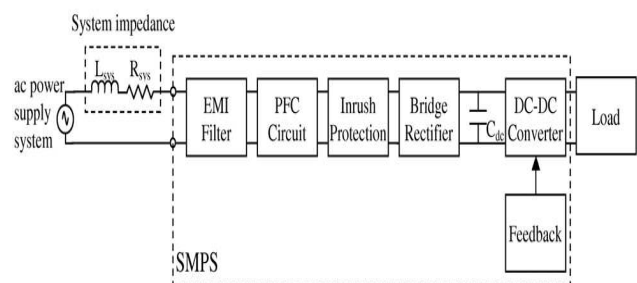


Fig. 1. General block diagram of SMPS load.

As the SMPS devices are non-linear loads, they are significant sources of harmonics in modern power supply systems. The presence of harmonics will have negative effects on the operation of power supply systems, including higher thermal stresses and overloading of system components (e.g. shortening of the lifetimes of transformers and cables), or increased neutral conductor currents[3]. Harmonics may also interact with supply system impedance, leading to distortions of the supply voltage (e.g. "flat-top" voltage waveforms). This paper presents some of the results of the ongoing work on providing more specific guidance (than what is presently available) about the harmonic emission characteristics of modern distribution system loads. More specifically, this paper considers the SMPS load category [3].

The direct effects of harmonics on equipment have been studied extensively, but what is the indirect effect of harmonics in the voltage supply on the voltage tolerance of equipment? The main objective of this paper is to analyze if harmonics in the voltage supply affect the sensitivity of equipment to voltage sags [4].

2.0 SINGLE PC AS A HARMONIC SOURCE

Power supply unit of a modern PC consists of input AC/DC converter with capacitive filtering on DC side. Simplified electrical scheme is shown in Fig.2. Current on AC side is determined with capacitor charging/discharging and therefore is impulse in nature. Such a wave shape is far from sinusoidal, so harmonic distortion is high. This different values of THD_i resulting from different processing modes of the PC, explains variety of the reported THD_i in references: 79.3% [12], 100-120% [9], 100% [10], 110% [5], 119% [19], 118-122% [6], 140% [1].

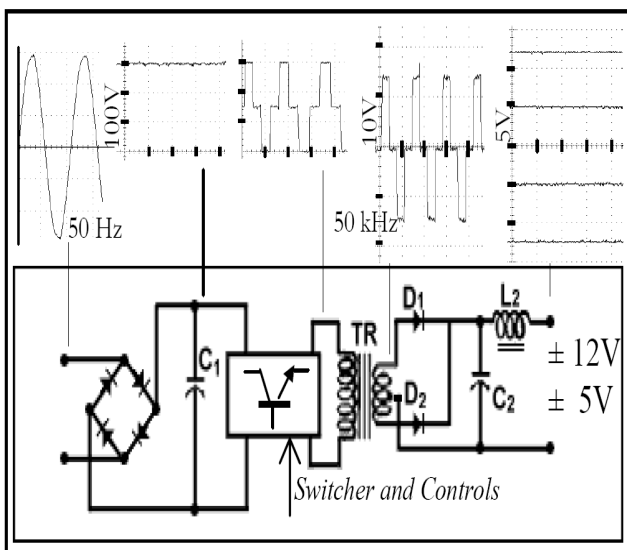


Figure 2. Simplified representation of a PC power supply unit (below) and characteristic wave-shapes (above).

3.0. CLASSIFICATION AND MODELLING OF SMPS LOADS

3.1 Classification of SMPS Loads

Harmonic legislation in [5] stipulates that electronic loads with rated active power less than or equal to 75 W do not need to satisfy any of the prescribed harmonic emission limits. Therefore, SMPS load category is divided/classified in this paper into low-power (≤ 75 W) and high-power (> 75 W) sub-categories (i.e. types) of SMPS load. The general structure (i.e. circuit topology) of low- and high-power SMPS loads are similar, except that low-power SMPS' will usually not have the power factor correction (PFC) circuit, Fig. 1, as they do not have to adhere to prescribed harmonic limits. High-power SMPS loads will utilise one of two general variants of PFC circuits: passive-PFC (p-PFC), or active- PFC (a-PFC). SMPS with a-PFC use an additional dc-dc converter to shape input current into a sinusoidal waveform. Devices with p-PFC, on the other

hand, include a relatively large inductor in the current conduction path. As an inductor will oppose the change of current, this will “smooth” the input current waveform, effectively widening input current pulses and therefore reducing its harmonic content. The SMPS' with a-PFC use more sophisticated circuits, and inject only a (very) low-level of harmonics. This assertion is additionally strengthened with the fact that p-PFC type of SMPS load is more common, as it is considerably cheaper to implement [6]. It should be noted, however, that as the cost of power electronic circuits falls, it is expected that the contribution of a-PFC type of SMPS load will increase. In this paper, the term “high-power SMPS” refers to SMPS devices with p-PFC and rated power > 75 W, while term “low-power SMPS” refers to SMPS devices with no-PFC and rated power 75 W.

3.2. Equivalent Circuit Model of SMPS Load

During the steady-state operation, both low and high power types of SMPS load can be represented by the equivalent circuit given in Fig. 3.

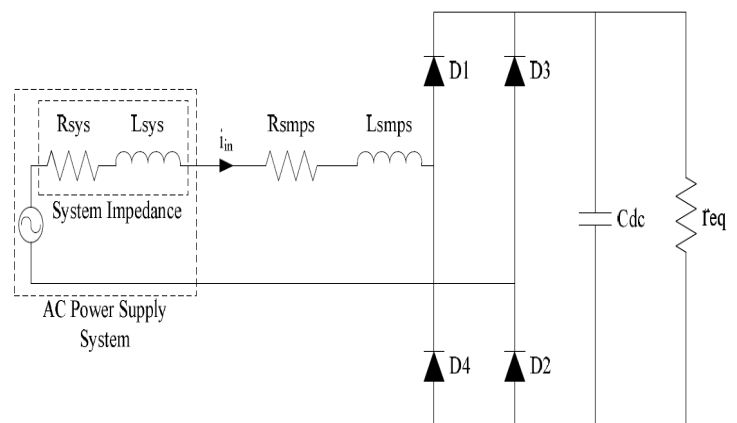


Fig. 3. Equivalent circuit model of SMPS load.

In Fig.3, L_{sys} and R_{sys} represent the system impedance (Z_{sys}), while R_{SMPS} and L_{SMPS} represent the sum of all resistances and inductances in the SMPS conduction path. Resistance r_{eq} is the “equivalent load resistance”, which represents dc-dc converter and the dc load supplied by the SMPS. This equivalent load resistance is defined as ([7]):

$$r_{eq} = \frac{v_{dc}^2}{P_{rated}} \quad (1)$$

where: v_{dc} is the instantaneous value of the dc link voltage and P_{rated} is the rated power of the modelled SMPS device. Further details on the implemented equivalent circuit model are given in [8].

3.3. Parameters of the Equivalent Circuit SMPS Model

Table I lists per-unit (pu) parameters of equivalent circuit SMPS model (based on the values identified from the actual SMPS devices), which have been shown to represent generic SMPS load in [9].

TABLE I
SMPS GENERIC CIRCUIT/MODEL VALUES, [9]

Model Parameter	SMPS type	
	Low-power	High-power
RSMPS [pu]	0.00142	0.00709
XCdc [pu]	0.036	0.036
XLSMPS [pu]	-	0.0371

Although system impedance is not part of the model, it is used to represent the power supply system to which SMPS load, together with the other loads, is connected at the point of common coupling (PCC), Fig. 4. In this paper, the impedance of the lines/conductors connecting loads to PCC is assumed to be negligible. The nominal and maximum values of system impedance used in this paper are taken from [10], while minimum system impedance value is estimated based on these two specified values, Table II.

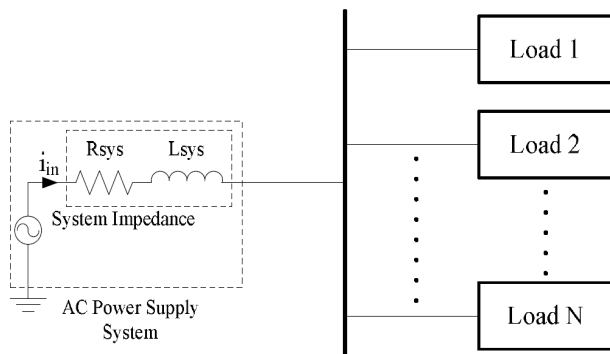


Fig. 4. Aggregate load connected to low-voltage network

TABLE II
SYSTEM IMPEDANCE VALUES, [10]

Value	System Impedance [Ω]	R _{sys} [Ω]	L _{sys} [mH]
Min	Z = 0.12 + j0.11	0.12	0.35
Nom	Z = 0.25 + j0.23	0.25	0.73
Max	Z = 0.46 + j0.45	0.46	1.43

4.0 PARAMETER VARIATION

Although the described generic equivalent circuit SMPS model can be used to represent some important characteristics of the aggregate SMPS load (e.g. their aggregate active and reactive power demands [9]), it does not have the ability to correctly model harmonic cancellation between the individual SMPS loads.

4.1. Resistance RSMPS

The resistance of the SMPS (R_{SMPS}) is dominated by the resistance of the negative temperature coefficient (NTC) thermistor used for inrush current protection. Although resistors generally have a much smaller tolerance range, typically around ±1 %, the range applied in the analysis in this paper is taken as ±20 %, in order to correctly represent different types of components and different operating temperature regions. A uniform distribution is taken for R_{SMPS} to allow for a more random variance in this parameter. The influence of R_{SMPS} on harmonic emission of low power SMPS load is small, Fig. 5, but still more significant than in case of high-power SMPS', Fig. 6. This is because the large inductor present in high-power SMPS with p-PFC will dominate the high-power device input impedance [10].

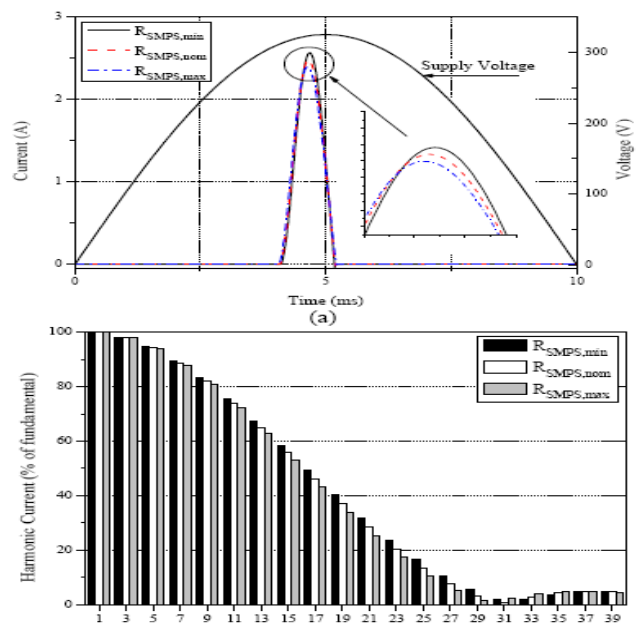


Fig. 5. Influence of resistance (R_{SMPS}) on low-power SMPS:

- a) instantaneous current waveform b) magnitudes/amplitudes of current harmonics

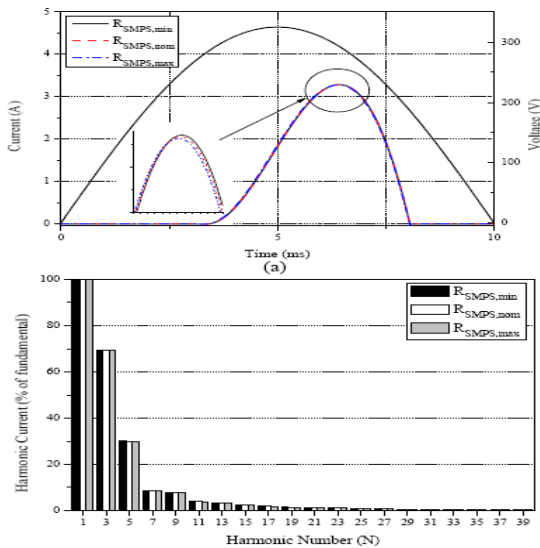


Fig. 6. Influence of resistance (Rsm) on high-power SMPS:a) instantaneous current waveform b) magnitudes/amplitudes of current harmonics

4.2. Capacitance Cdc

The capacitor (Cdc) in SMPS devices must be large enough to allow SMPS to ride-through a voltage interruption of up to 10ms [11]. However, if the voltage interruption starts just before the Cdc is about to charge, then a 10ms interruption corresponds to a 20ms interruption for a fully charged capacitor. A common industry practice is to select the value of Cdc to satisfy a hold-up time of 23ms, which is 20ms hold-up time plus a safety margin, [12]. In order to calculate the size of Cdc necessary to achieve a particular hold-up time, the rated power of the SMPS and the minimum operational input voltage of the dc-dc converter in the SMPS must both be known. Although the exact value of minimum operating voltage will be dependent on the specific dc-dc converter, values of around 80 V are common [13]. Therefore, the selected value of Cdc should be large enough to maintain dc link voltage greater than 80 V. This was simulated using full circuit SMPS model in [14], where the value of Cdc was adjusted at each rated power to just satisfy the hold up criteria, Fig. 7.

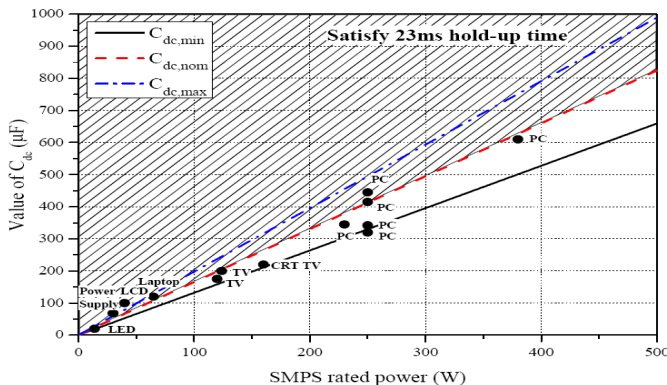


Fig. 7. Range of typical values of Cdc found in SMPS load.

The values of Cdc obtained in simulations with full circuit SMPS model are compared with the values of Cdc found after the inspection of actual SMPS', and with data from manufacturer's specifications in Fig. 6. Figure 6 shows good agreement between simulations and identified or measured values. This allowed to specify a nominal pu value of Cdc:

$$X_{C_{dc},pu} = \frac{1/\omega C_{dc}}{(V_{phase}^2 / P_{rated})} \approx 0.036 pu \quad (2)$$

where: Vphase is the rms value of the supply voltage, Prated is the rated power of the modelled SMPS and ω is the angular frequency of the supply voltage.

Actual values of capacitors in SMPS circuits may vary based on their manufacturing tolerance, which is typically ±20% for electrolytic-type capacitors used in low-voltage single-phase SMPS devices [13].

4.3. Inductance Lsm

The inductance (Lsm) of the SMPS device is dominated by the value of the PFC inductor selected to satisfy harmonic legislation. Accordingly, this model parameter is only present in high-power SMPS load. To determine the value of Lsm inductor to satisfy harmonic legislation, the inductor size was adjusted until the harmonic limits were just met at each rated power using a detailed full-circuit SMPS model. This was repeated for the three values of Cdc identified in the previous section, which were found to have only a small effect. The minimum value (for just satisfying requirements in [5]) is given by (3).

$$X_{L_{sm},pu} = \frac{\omega L_{sm}}{(V_{phase}^2 / P_{rated})} \approx 0.0315 pu \quad (3)$$

It was found that this minimum value was approximately 15% lower than measured values. This generally agrees with typical inductor tolerances, usually given as ±10% [13] and ±15% [14].

4.4. Variations in SMPS Operating Conditions

Rated power of an SMPS' device is the maximum power that the device can safely provide during the normal operation. For the majority of SMPS applications, however, it is highly unlikely that the device will continuously provide this power. During the normal operation, power demand of the SMPS will change based on the actual loading conditions at its dc output(s). It has been found that the power consumption of a typical low-voltage SMPS (e.g. TV, PC, monitor etc.) will depend upon the specific operating mode of the device. Therefore, it is important to consider how loading conditions of an SMPS device will influence harmonic content of its input current. The most dominant type of SMPS load in residential and commercial load sectors are PC's and monitors[15]. To determine the

range of their loading conditions (P_{load}), several of these devices were measured during typical operations.

4.5 Voltage Tolerance Curve of Equipment Under Non sinusoidal Conditions:

A way to characterize the behavior of equipment to voltage sags is to use voltage-tolerance curves. The first voltage-tolerance curve, the CBEMA curve-which was initially applied to data processing equipment-shows that the sensitivity of equipment is very dependent on the duration of the voltage sag. This voltage-tolerance curve is an important part of IEEE standard 1346 is shown in Fig.8

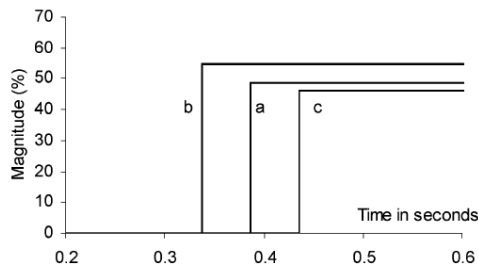


Fig. 8.Limits of the voltage tolerance of a PC in different supply conditions

IEC standard 61000-4-11 describes two possible test configurations for supply simulation to show the behavior of equipment under different supply conditions. The first one uses two transformers with variable output voltages, and the second uses waveform generators and power amplifiers. Although the second configuration allows testing equipment in the context of frequency variations and harmonics, no references are made in the literature about the voltage tolerance of equipment in these conditions.

5.0 SIMULATION RESULTS

The circuit presented in Fig.3 was simulated by using MAT LAB. Fig. 9(a) and (b) shows an effect of non linear load (PC model) on source voltage and harmonic spectrum respectively. The voltage harmonics produces the total harmonic distortion (THD) is 73.6% which will effect more when a large number of PCs are connected. Fig. 10 (a) and (b) shows source current and harmonic spectrum respectively. The current harmonics produces the total harmonic distortion (THD) is 108.53% .

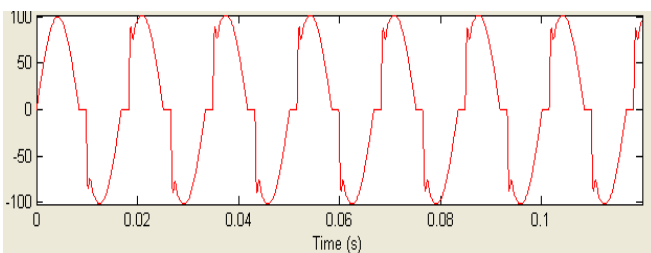


Fig 9 (a) Source voltage of pc model

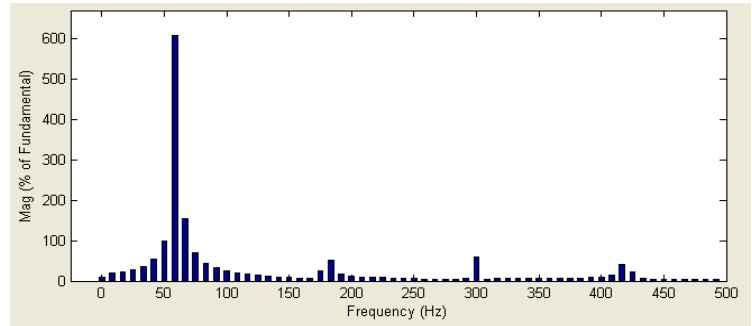


Fig 9 (b) Harmonic spectrum of source voltage

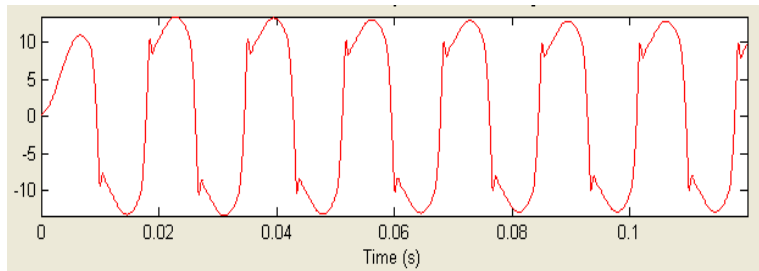


Fig. 10 (a) Source current of PC model

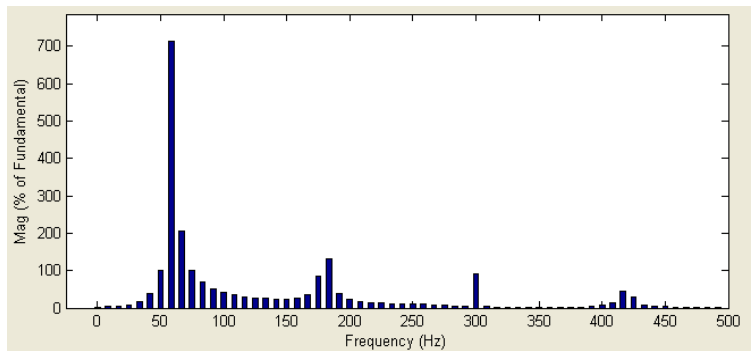


Fig. 10 (b) Harmonic spectrum of source current of PC model

6.0. CONCLUSIONS

This paper presents results of a detailed investigation into the harmonic characteristics of modern switch-mode power supply (SMPS) loads. The number of these devices has substantially increased over the last few decades, and it is, therefore, important to correctly analyse their harmonic characteristics when they are represented as an aggregated load. Using previously developed equivalent circuit SMPS models and this paper analyses influence of typical ranges of variations of SMPS circuit's parameters on harmonic emission between same-type and mixed-type SMPS aggregate load. Additionally, the paper also analyses the effects of variations in power demands of SMPS' during their normal operation and voltage tolerance limits to know behaviour of equipment. Simulation results were shown how non linear load (PC) effects source voltage and current. One single PC produces current harmonic distortion (THD) 108.53%.

7.0. REFERENCES

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